www.einfochips.com

JOB DESCRIPTION, ROLE & RESPONSIBILITES

POSITION TITLE: Senior Engineer/Engineer – Design For Testability
LOCATION: Ahmedabad/Bangalore.

ROLE & RESPONSIBILITIES

- Incumbent will be responsible for Scan insertion and validation, BIST, MBIST insertion and validation, ATPG, IP Tests and Pattern validation w/wo Timing, DFT mode timing Analysis and sign off.
- Be responsible for a comprehensive DFT plan
- Incumbent to work with DFT and cross functional teams
- To architect and implement solutions for Scan and built-in self-test (Memory and Logic BIST) circuitry to test devices in the field

ESSENTIAL SKILLS & EXPERIENCE

- Minimum 4 year's experience in DFT Fundamentals.
- Strong fundamentals on DFT and ASIC cycle.
- Sound expertise in Tcl, Perl, Shell scripting. Technically sound & good team player
- Hands-on experience with DFT implementation using standard EDA and flow is a must.
- Experience on latest technology (28nm,16nm,7 nm)

EDUCATION BACKGROUND

- B.E./ B.S./ B.Tech/ M.S./ M.Tech in VLSI/Electronics/Electrical/Computer/Instrumentation Engineering.

ABOUT eInfochips (An Arrow Company):

eInfochips, an Arrow company (A $30B, NASDAQ listed (ARW); Ranked #102 on the Fortune List), is a leading global provider of product engineering and semiconductor design services. 25+ years of proven track record, with a team of over 2500+ engineers, the team has been instrumental in developing over 500+ products and 40M deployments in 140 countries. Company's service offerings include Silicon Engineering, Embedded Engineering, Hardware Engineering & Digital Engineering services. eInfochips services 7 of the top 10 semiconductor companies and is recognized by NASSCOM, Zinnov and Gartner as a leading Semiconductor service provider.